AMENDMENTS TO THE CLAIMS

1-13. (cancelled)

14. (currently amended) A Gray code counter for outputting a code word comprising:

~~a clock generator for outputting a clock signal; and~~

a plurality of bit counts coupled serially, ~~a first~~ at least one bit unit comprising:

an XOR gate for receiving a first input signal;

an AND gate for receiving a reverse second input signal and outputting a first output signal;

an OR gate for receiving a second input signal and outputting a second output signal; and

a flip flop having a signal input coupled with an output of the XOR gate, and a signal output coupled respectively with inputs of the XOR gate, the AND gate and the OR gate for outputting a bit output signal according to ~~the~~ a clock signal,

wherein ~~the Gray code counter is composed of a plurality of the first bit units connected serially, and~~ the code word comprises the bit output signal.

15. (currently amended) ~~A Gray code counter comprising~~ The Gray code counter of claim 14, wherein at least one of the bit units further comprises:

~~a clock generator for outputting a clock signal; and~~

~~a first bit unit comprising:~~

~~an XOR gate for receiving a first input signal;~~

~~an AND gate for receiving a reverse second input signal and outputting a first output signal;~~

~~an OR gate for receiving a second input signal and outputting a second output signal;~~

~~a flip flop having a signal input coupled with an output of the XOR gate, and a signal output coupled respectively with input ends of the AND gate and the OR gate, for outputting a Gray code bit output signal~~

~~according to the clock signal; and~~

~~a second bit unit comprising:~~

~~an XOR gate for receiving a third input signal;~~

~~an AND gate for receiving a reverse fourth input signal and outputting a third output signal;~~

~~an OR gate for receiving a fourth input signal and outputting a fourth output signal;~~

~~a flip flop having a signal input coupled with an output of the XOR gate, and a signal output, for outputting a Gray code bit output signal according to the clock signal; and~~

an XNOR gate having a first input coupled to the signal output of the flip flop for receiving the bit output signal, a second input for receiving a third input signal, and an output ~~connected~~ coupled to input ends of the AND gate and the OR gate ~~respectively, for receiving a fifth input signal and the Gray code bit output signal;~~.

16. (new) A method for generating a Gray code sequence having N code words comprising:

determining an exponent number M, wherein 2^M>N;

generating a full length Gray code sequence having 2^M code words;

generating a first bit switch sequence having 2^M-1 elements, wherein each element of the first bit switch sequence represents the difference between one of the code words and an adjacent code word of the full length Gray code sequence;

deleting 2^M-N elements of the first bit switch sequence according to a bit switching sequence property to generate a second bit switch sequence having N-1 elements; and

generating the Gray code sequence having N code words according to the second bit switch sequence, wherein each element of the second bit switch sequence represents the difference between one of the code words and an adjacent code word of the Gary code,

wherein the bit switching sequence property indicates that there is at least one

element that appears an odd number of times in the bit switch sequence.

17. (new) The method of claim 16, wherein the full length Gray code sequence further comprises a first half and a second half, wherein the first half and the second half are mirror images of one another with the exception of the most significant bits of the code words.

18. (new) The method of claim 17, wherein the first bit switch sequence further comprises a middle element, and the first bit switch sequence is divided into a first ordered sub-set and a second ordered sub-set by the middle element, wherein the first ordered sub-set and the second ordered sub-set are the same size.

19. (new) The method of claim 18, wherein if 2^M-N is an even number, the second bit switch sequence is generated by deleting (2^M-N) /2 element(s) from the first ordered sub-set and (2^M-N) /2 element(s) from the second ordered sub-set of the first bit switch sequence, wherein the position of the deleted element(s) in the first ordered sub-set corresponds to the position of the deleted element(s) in the second ordered sub-set.

20. (new) The method of claim 19, wherein the value of each deleted element of the first ordered sub-set is the same as the value of the corresponding deleted element of the second ordered sub-set.

21. (new) The method of claim 19, wherein the position of each deleted element of the first ordered sub-set is the same as the position of the corresponding deleted element of the second ordered sub-set.

22. (new) The method of claim 19, wherein the position of each deleted element of the first ordered sub-set is the mirror image of the position of the corresponding deleted element of the second ordered sub-set.

23. (new) The method of claim 18, wherein if 2^M-N is an odd number, the second bit switch sequence is generated by deleting (2^M-N-1) /2 first element(s) from the first ordered sub-set and (2^M-N-1) /2 second element(s) from the second ordered sub-set of the first bit switch sequence, wherein the position of the deleted element(s) in the first ordered sub-set corresponds to the position of the deleted element(s) in the second ordered sub-set, and then deleting one more element from the remaining elements of the first bit switch sequence.

24. (new) The method of claim 23, wherein the value of each first deleted element of the first ordered sub-set is the same as the value of the corresponding second deleted element of the second ordered sub-set.

25. (new) The method of claim 23, wherein the position of each first deleted element of the first ordered sub-set is the same as the position of the corresponding second deleted element of the second ordered sub-set.

26. (new) The method of claim 23, wherein the position of each first deleted element of the first ordered sub-set is the mirror image of the position of the corresponding second deleted element of the second ordered sub-set.

27. (new) A method for generating a Gray code sequence having N code words

comprising:

determining an exponent number M, wherein 2^M>N;

generating a first bit switch sequence having 2^M-1 elements according to a bit switching sequence property, wherein the value of each element of the first bit switch sequence is an integer number ranging from 1 to M;

deleting 2^M-N element of the first bit switch sequence according to the bit switching sequence property to produce a second bit switch sequence; and

generating the Gray code sequence having N code words according to the second bit switch sequence, wherein each element of the second bit switch sequence represents the difference between one of the code words and an adjacent code word of the Gary code sequence;

wherein the bit switching sequence property indicates that there is at least one element that appears an odd number of times in the bit switch sequence.

28. (new) The method of claim 27, wherein the first bit switch sequence further comprises a middle element, and the first bit switch sequence is divided into a first ordered sub-set and a second ordered sub-set by the middle element, wherein the first ordered sub-set and the second ordered sub-set are the same size.

29. (new) The method of claim 28, wherein if 2^M-N is an even number, the second bit switch sequence is generated by deleting (2^M-N) /2 element(s) from the first ordered sub-set and (2^M-N) /2 element(s) from the second ordered sub-set of the first bit switch sequence, wherein the position of the deleted element(s) in the first ordered sub-set corresponds to the position of the deleted element(s) in the second ordered sub-set.

30. (new) The method of claim 29, wherein the value of each deleted element of the first ordered sub-set is the same as the value of the corresponding deleted element of the second ordered sub-set.

31. (new) The method of claim 29, wherein the position of each deleted element of the first ordered sub-set is the same as the position of the corresponding deleted element of the second ordered sub-set.

32. (new) The method of claim 29, wherein the position of each deleted element of the first ordered sub-set is the mirror image of the position of the corresponding deleted element of the second ordered sub-set.

33. (new) The method of claim 28, wherein if 2^M-N is an odd number, the second bit switch sequence is generated by deleting (2^M-N-1) /2 first element(s) from the first ordered sub-set and (2^M-N-1) /2 second element(s) from the second ordered sub-set of the first bit switch sequence, wherein the position of the deleted element(s) in the first ordered sub-set corresponds to the position of the deleted element(s) in the second ordered sub-set, and then deleting one more element from the remaining elements of the first bit switch sequence.